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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/695,102

10/28/2003

Arya R. Behzad

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06/15/2005

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EXAMINER

CHOE, HENRY

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

26

Office Action Summary	Application No. 10/695,102	Applicant(s) BEHZAD ET AL.	
	Examiner Henry K. Choe	Art Unit 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5 and 7 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Mitzlaff (Fig. 2).

Mitzlaff (Fig. 2) discloses an amplifier circuit comprising the method steps of dividing (203) the signal (RF INPUT) to be amplified into a plurality of signals (horizontal output of 203 and vertical output of 203), coupling each of the divided signals (horizontal output of 203 and vertical output of 203) into an amplifier circuit (205, 207) having a power source (DC), enabling (211, 213) a selected amplifier (205 or 207) to select a programmable gain, and removing (211, 213) the power source (DC) from a plurality of non-selected amplifiers (205, 207).

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Walker (Fig. 1).

walker (Fig. 1) discloses an amplifier circuit comprising the method steps of dividing (a node between the impedance matching circuits 14 and 16) the signal (INPUT) to be amplified into a plurality of signals (a signal going into the matching circuit 16 and a signal going into the matching circuit 17), coupling each of the divided signals (a signal going into the matching circuit 16 and a signal going into the matching circuit

17) into an amplifier circuit (M1, M2) having a power source (GATE BIAS), enabling (GATE BIAS AND R3) a selected amplifier (M1 or M2) to select a programmable gain, and removing the power source (GATE BIAS, BIAS) from a plurality of non-selected amplifiers (M1 or M2).

Claims 5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Schwent et al (Fig. 1).

Regarding claim 5, Schwent et al (Fig. 1) discloses an amplifier circuit comprising the method steps of dividing (a node between the input terminal and inputs of 200 and 201) the signal (INPUT RF SIGNAL) to be amplified into a plurality of signals (a signal going into the amplifier 200 and a signal going into the amplifier 201), coupling each of the divided signals (a signal going into the amplifier 200 and a signal going into the amplifier 201) into an amplifier circuit (200, 201) having a power source (VS), enabling (when the switches CS1-CS3 are closed) a selected amplifier (200 or 201) to select a programmable gain, and removing the power source (VS) from a plurality of non-selected amplifiers (200 or 201).

Regarding claim 7, the removing of the power source (VS) from the plurality of non-selected amplifiers (200 or 201) includes disconnecting a power supply connection from the plurality of non-selected amplifiers (200 or 201).

Allowable Subject Matter

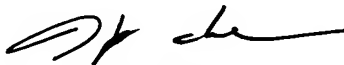
Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent number (5,451,907) is the parallel amplifiers with the bias circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.


HENRY CHOE
PRIMARY EXAMINER

#1023